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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,566	07/21/2004	Deok-kee Kim	FIS920040057 (00750489AA)	4565

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WHITHAM, CURTIS & CHRISTOFFERSON & COOK, P.C.
11491 SUNSET HILLS ROAD
SUITE 340
RESTON, VA 20190

EXAMINER	
ARENA, ANDREW OWENS	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 10/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/710,566	KIM ET AL.	
	Examiner	Art Unit	
	Andrew O. Arena	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *07/21/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4, 7-12, and 14-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Hummler (US 6,620,677).

RE claim 1, Hummler discloses (Fig 1-11) a method for manufacture of an integrated circuit (col 1 ln 15-17) having structures formed in respective first (16) and second (18) areas thereon, said method comprising steps of:

reducing height of structures in said first (46 in Fig 7A – 48 in Fig 8) and second (39 in Fig 1A – 40 in Fig 2A) areas,

removing a material from said first (col 6 ln 52-54) and second areas (col 5 ln 50) sequentially, and

replacing said material (Fig 9) removed from said first and second areas with a first material (50) in said first area and a second material (50) in said second area, respectively, one of said first and second materials being an isolation material (col 6 ln 66),

using a polysilicon block-out mask (44; col 6 ln 17-21) to protect said second area to separately process (col 6 ln 29-35) the first area,

planarizing (col 7 ln 5) said first and second materials to provide a planar surface, and

completing said integrated circuit (col 7 ln 54-55).

RE claim 2, Hummler discloses said isolation material is an array top oxide (col 7 ln 1)

RE claim 3, Hummler discloses a polysilicon hard mask is used to mask said second area (col 6 ln 17-21, 26-28).

RE claim 4, Hummler discloses said polysilicon hard mask comprises a single layer (44) of polysilicon.

RE claim 7, Hummler discloses depositing a nitride liner (42; col 6 ln 10-12) prior (Fig 8-9) to said step of depositing said isolation material (50).

RE claim 8, Hummler discloses equalizing (average) heights of structures (48, 34, 38) in said first and second areas by etching prior to said planarizing step.

The above rejection of claim 8 relies on interpreting the term "equalizing" consistent with applicant's disclosure, e.g. Fig 16 and spec ¶50 ln 5-6.

RE claim 9, Hummler discloses said integrated circuit is a memory device, said first area is a memory array area and said second area is a support area (col 5 ln 9-11).

RE claim 10, Hummler discloses said integrated circuit includes an embedded memory, said first area is a memory array area and said second area is a support area (col 5 ln 9-11).

RE claim 11, Hummler discloses wherein said planarizing step includes:

applying a planarizing material (ARC) over said structures in said first and second areas and said first and second materials, and non-selectively etching (RIE) said planarizing material, said first material, said second material and said structures (col 7 ln 5-10).

RE claim 12, Hummler discloses a method for planarizing a surface having structures formed thereon and an additional layer (50) of material covering said surface and said structures formed on said surface, said method including steps of

applying a planarizing material (ARC) to said layer of material to form a substantially planar surface above said surface having structures formed thereon, and

performing a non-selective etching (RIE) from said substantially planar surface to a said predetermined structure formed thereon col 7 ln 5-10).

RE claim 14, Hummler discloses said structures have a first average height in a first area of said surface and structures of a second average height greater than said first average height in a second area of said surface (Fig 8), said method comprising the further steps of:

etching said structures of said second average height to an average height substantially equal to said first average height (substantially equal interpreted to include slightly greater),

subsequent to said etching step, applying a planarizing material (ARC) to said first and second areas of said surface and covering said structures remaining in said

first and second areas whereby a surface of said planarizing material is substantially planar (col 7 ln 5), and

performing said step of non-selectively etching (RIE) said planarizing material and structures overlaid by said planarizing material to completely remove said planarizing material and form a planar surface (no ARC in Fig 10).

RE claim 15, Hummler discloses said step of non-selective etching includes removal of a nitride liner (Fig 9: 42) below said layer of material (col 7 ln 7).

RE claim 16, Hummler discloses a method for planarizing a surface of a body of material, said method including steps of:

applying a planarizing material (ARC) to said body of material to form a substantially planar surface, and

performing a non-selective etching (RIE) from said substantially planar surface to a point on or within said body of material (col 7 ln 5-7).

RE claim 17, Hummler disclose the method in combination with a top oxide early process for forming an integrated circuit (col 3 ln 41-43, col 8 ln 12-20).

RE claim 18, Hummler the method in combination with a top oxide nitride process for forming an integrated circuit (col 3 ln 41-43, col 8 ln 12-20).

RE claim 19, Hummler the method in combination with a top oxide late process for forming an integrated circuit (col 3 ln 41-43, col 8 ln 12-20).

RE claim 20, Hummler discloses adjusting height of a structure on a differentiated area of said body of material (e.g. etches of Fig 2A, 6A, or 8).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5 and 6 are rejected under 35 USC 103(a) as being unpatentable over Hummler.

RE claims 5 & 6, Hummler discloses said second area is etched while said first area is not (Fig 2A, col 5 ln 49-50, 57-65).

Hummler differs from the claimed invention only in not expressly disclosing a polysilicon hard mask is used to mask said first area.

Hummler discloses etched portions of the second area are made of the same material (an insulator, col 5 ln 30-31, 41-42) as non-etched portions of the first area and discloses a similar etch using a polysilicon hard mask (Fig 7A-8, col 6 ln 17-21, 29-35) that comprises a single layer (44) of polysilicon.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that a polysilicon hard mask is used to mask said first area, and that said polysilicon hard mask comprises a single layer of polysilicon; at least to prevent etching the first area using a known suitable material.

Claim 13 is rejected under 35 USC 103(a) as being unpatentable over Hummler as applied to claim 12 above, and further in view of Gustafson (US 6,837,965).

RE claim 13, Hummler discloses (Fig 11) determining termination of said step of non-selective etching (col 7 ln 40-42: stopping inherently done by determining stopping).

Hummler differs from the claimed invention only in not expressly disclosing end point detection.

Gustafson discloses end point detection (col 1 ln 29) during the etch of a bulk material of a substrate (col 1 ln 24).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that Hummler, in view of Gustafson, include performing end point detection to detect a material interface for determining termination of said step of non-selective etching; at least to etch only as much as desired.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew O. Arena whose telephone number is (571) 272-5976. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Andrew O Arena
2 October 2006

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800